Soham Gandhi

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EXPERIENCE

Texas Instruments | *Digital IC Design Intern* | Santa Clara, CA May 2024 – Aug 2024

- Collaborated with analog, design verification, and systems teams to design a modular chip, slashing costs by 50% and reducing SoC package size by 75% to meet customer specifications.
- Executed RTL simulations and debugging for automotive SerDes chips using Cadence and SimVision, optimizing audio and video functionalities.
- Architected a high-speed FIFO in SystemVerilog with prefetchers and single-port RAM, boosting speed 50%.

Texas Instruments | *Validation Engineering Intern* | Santa Clara, CA May 2023 – Aug 2023

- Collaborated with an external company to develop a lab methodology that emulated automotive high-speed SerDes cables using a programmable Artek Variable ISI channel, cutting SerDes link testing time by 60%.
- Developed automation drivers for Keysight PNA S-parameter measurements and Artek Variable ISI Channel controls, reducing setup time by 90% for ADAS and IVI chip testing.
- Automated ASIC setup and testbench configuration using Python, reducing validation time and effort by 3x.

General Dynamics | *Software Engineering Intern* | Fair Lakes, VA May 2022 – Aug 2022

- Streamlined CentOS configuration setup by researching package dependencies, reducing setup size by 80%.
- Automated CentOS deployment over NFS using DHCP and TFTP, cutting deployment time by 50%.

EDUCATION

Virginia Tech Aug 2021 **–** May 2025

Dual B.S. in Computer & Electrical Engineering **GPA:** 3.92

Minor in Computer Science

Relevant Coursework: Digital Design, Adv Computer Architecture, Digital & Mixed Signal System Testing, Artificial Intelligence, Computer Vision, Digital Image Processing

Awards: Calhoun Scholar, Dean's List, HackViolet 2023 (Best Innovation Hack), 2022 CHCI Symposium (3rd)

Thomas Jefferson High School for Science and Technology Aug 2017 **–** June 2021

PROJECTS

FPGA Neural Network | *Developer* Jun 2024 – Present

- Developed Python scripts to convert TensorFlow models into Verilog boosting performance by 50%.
- Explored methods to implement transfer functions using 32-bit floating-point numbers for precision.
- Implemented generate blocks & parameterization, to support multiple activation functions and layer sizes.

ARM Pointer Authentication Security | *Research Assistant* Jun 2024 – Present

- Enhanced the Rocket Chip architecture, developed by UC Berkley, by integrating a custom pointer encryption algorithm that executes within a single CPU clock cycle.
- Engineered a hardware-level implementation of the PRINCE encryption algorithm.
- Working towards publication to present advancements in pointer security and encryption techniques.

BEARHW (sPACtre) | *Research Assistant* Aug 2023 – May 2024

- Analyzed computer specifications and replicated 4 Spectre variant side-channel attacks on M1 Mac ARM architecture using C and Assembly, contributing to pending conference publication.
- Investigated Spectre side-channel vulnerabilities and proposed mitigation strategies.

Latis | *Founder & Developer* Nov 2022 – May 2023

- Built a decentralized update platform using blockchain, reducing vulnerability to DDoS attacks by 70%.
- Developed a web application to streamline manufacturer-OEM interactions via smart contracts, improving update times by 50%.
- Led an 8-member team in successful market research and investor pitch presentations.

SKILLS

Programming Languages: SystemVerilog, Verilog, C++, C, Python, Java, Bash, Git

Hardware Design: FPGA Design, ASIC Design, Digital IC Design, SerDes, Mixed-Signal Systems

Tools & Technologies: Cadence, SimVision, Quartus, ModelSim, TensorFlow, Keysight PNA